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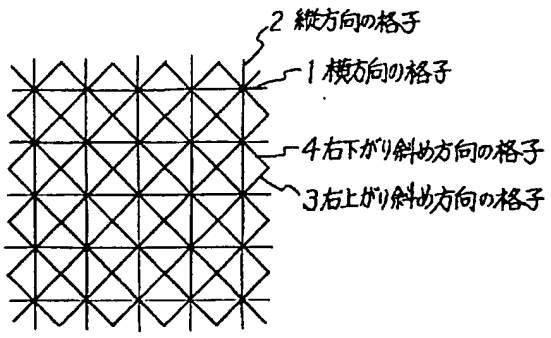
(54)【発明の名称】　半導体集積回路の自動レイアウト方法

(57)【要約】

【目的】　決められた格子の上を定められた配線層で配線するアルゴリズムを用いた半導体集積回路の自動レイアウト方法で配線した配線の長さを短かくする。

【構成】横方向の格子１および縦方向の格子２に加えて新たに斜め方向の格子３，４を設け、それぞれの格子上に主に使う配線層を定める。これにより配線すると、Ａ点Ｂ点間の配線パタン５、Ｃ点Ｄ点間の配線パタン６のようになる。

【効果】配線の長さを最大０．７倍に短かくすることができ、配線抵抗と配線容量が減るので動作速度が速くなる。



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【特許請求の範囲】

【請求項１】　少なくともひとつの横方向の格子上の配線に使う配線層と、少なくともひとつの縦方向の格子上の配線に使う配線層と、少なくともひとつの斜め方向の格子上の配線に使う配線層とを用いることを特徴とする半導体集積回路の自動レイアウト方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体集積回路の自動レイアウト方法に関し、特に決められた格子の上を定められた配線層で配線するアルゴリズムを用いた自動レイアウト方法に関する。

【０００２】

【従来の技術】従来の決められた格子の上を定められた配線層で配線するアルゴリズムを用いた半導体集積回路の自動レイアウト方法は、例えば図３に示すように、第１の配線層を主に横方向の格子１１上の配線に使い、第２の配線層を主に縦方向の格子１２上の配線に使っていた。さらに、３層以上の配線層を使う場合は、第３の配線層を第１の配線層と同一の横方向の格子１１上、第４の配線層を第２の配線層と同一の縦方向の格子１２上、というように順次割り当てて使っていた。

【０００３】図４は図３の格子に従って実際に配線したパタン図である。図４において、横方向に第１の配線層１５があり、縦方向に第２の配線層１６があり、各配線層１５，１６の接続パタン１７で電気的に接続されている。これらは、Ａ，Ｂ点，Ｃ，Ｄ点間の電気的接続をするための配線パタンである。

【０００４】

【発明が解決しようとする課題】このような従来の半導体集積回路の自動レイアウト方法では、たとえ３層以上の配線層を使っても横方向または縦方向の格子１１，１２上にしか配線しないので、配線層を増やしても配線がしやすくなるだけで、配線の長さはあまり短かくならないという問題点があった。

【０００５】本発明の目的は、前記問題点を解決し、配線の長さを短かくする半導体集積回路の自動レイアウト方法を提供することにある。

【０００６】

【課題を解決するための手段】本発明の半導体集積回路の自動レイアウト方法の構成は、少なくともひとつの横

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方向の格子上の配線に使う配線層と、少なくともひとつの縦方向の格子上の配線に使う配線層と、少なくともひとつの斜め方向の格子上の配線に使う配線層とを用いることを特徴とする。

【０００７】

【実施例】図１は本発明の一実施例で使用される配線格子図である。図１において、横方向の格子１と縦方向の格子２に加えて、右上がり斜め方向の格子３と右下がり斜め方向の格子４とを設定し、それぞれの格子１，２，３，４上の配線に主に使う配線層として、第１から第４の配線層を割り当てる。

【０００８】図２は図１の格子図を用いて配線パタンを行ったパタン図である。

【０００９】図２において、第１の配線層７，第２の配線層８，第３の配線層５，第４の配線層６とがあり、各配線層間の接続パタン９が接続点等に設けられている。

【００１０】図２では、Ａ点Ｂ点間，およびＣ点Ｄ点間を配線した例で、従来の図４と比べて、配線の長さが０．７～０．８倍に短かくなっている。

【００１１】

【発明の効果】以上説明したように、本発明は、従来の横および縦方向の格子上の配線に使う配線層に加えて、斜め方向の格子上の配線に使う配線層を用いることにより、配線の長さを最大０．７倍に短かくすることができ、配線抵抗と配線容量とが減るので、動作速度が速くなるという効果を有する。

【図面の簡単な説明】

【図１】本発明の一実施例の半導体集積回路の自動レイアウト方法で使用される配線格子図である。

【図２】図１の格子に沿って作成した配線パタン図である。

【図３】従来の自動レイアウト方法で使用される配線格子図である。

【図４】図３の格子に沿って作成した配線パタン図である。

【符号の説明】

１，１１　　横方向の格子

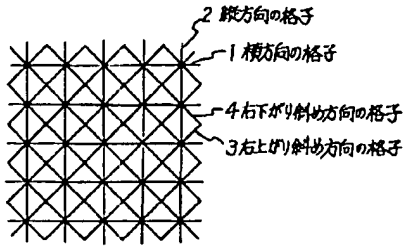
２，２２　　縦方向の格子

３　　右上がり斜め方向の格子

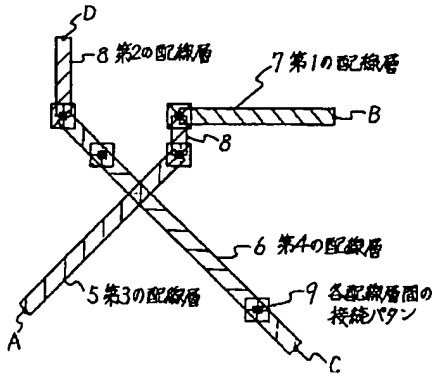
４　　右下がり斜め方向の格子

５，６，１５，１６　　２点間の配線パタン

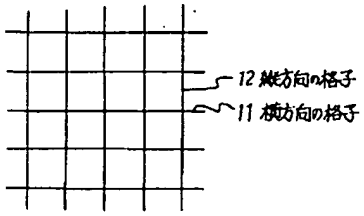
【図1】



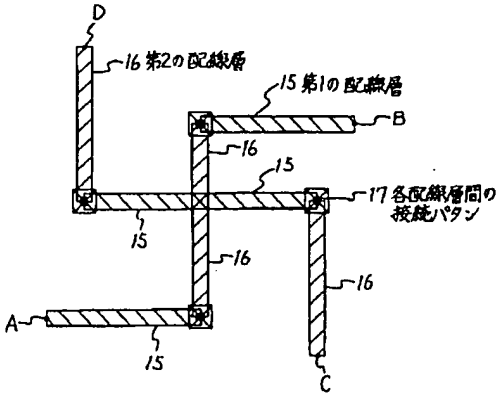
【図2】



【図3】



【図4】



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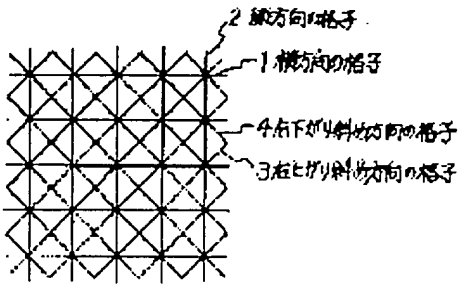
(54) AUTOMATIC LAYOUT METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PURPOSE: To make the length of wiring short by a method wherein, in addition to wiring layer which is used for wiring on lattices in the transverse and longitudinal directions in conventional cases, a wiring layer which is used for lattice-shaped wiring in the oblique direction is used.
CONSTITUTION: In addition to lattices 1 in the transverse direction and lattices 1 in the longitudinal direction, lattices 3 in the rightward ascending oblique direction and lattices 4 in the rightward descending oblique direction are set, they are used as wiring layers which are used mainly for wiring on the respective lattices 1, 2, 3, 4, and a first inter-connection layer to a fourth wiring layer are allotted. Thereby, the length of the wiring can be shortened to 0.7 times at the most, and the wiring resistance and wiring capacitance are reduced. As a result, the operating speed of the title integrated circuit can be made fast.



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[Date of request for examination]

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		9169-4M		C
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(54) [Title of Invention]

Aut matic Lay ut Meth d f r Semicoɹductor Integrated Circuits

(57) [Abstract]

[Purpose]

To shorten the wiring length of wiring made by an automatic layout method for semiconductor integrated circuits using an algorithm that implements wiring on decided lattice members in determined wiring layers.

[Constitution]

In addition to horizontal-direction lattice members 1 and vertical-direction lattice members 2, diagonal lattice members 3 and 4 are newly provided, and the wiring layer primarily used is determined on those lattice members. When wiring is implemented in this manner, the result is a wiring pattern 5 between point A and point B, and a wiring pattern 6 between point C and point D.

[Benefits]

It is possible to shorten the wiring length by a maximum factor of 0.7, whereupon wiring resistance and wiring capacitance are reduced so that the operating speed is increased.

[Claims]

[Claim 1] An automatic layout method for semiconductor integrated circuits that employs a wiring layer using wiring on at least one horizontal-direction lattice member, a wiring layer using wiring on at least one vertical-direction lattice member, and a wiring layer using wiring on at least one diagonal-direction lattice member.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention concerns an automatic layout method for semiconductor integrated circuits, and more particularly concerns an automatic layout method that uses an algorithm that implements wiring on decided lattice members in determined wiring layers.

[0002]

[Prior Art]

In a conventional automatic layout method for semiconductor integrated circuits that uses an algorithm that implements wiring on decided lattice members in determined wiring layers, as diagrammed in Fig. 3, for example, a first wiring layer is primarily used in wiring on a horizontal-direction lattice member 11, while a second wiring layer is primarily used in wiring on a vertical-direction lattice member 12. Furthermore, when three or more wiring layers are used, [the additional layers] are allocated in sequence, the third wiring layer being made on the same horizontal-direction lattice member 11 as the first wiring layer, and the fourth wiring layer being made on the same vertical-direction lattice member 12 as the second wiring layer.

[0003]

Fig. 4 is a diagram of a pattern actually wired following the lattice diagrammed in Fig. 3. In Fig. 4, there are a first wiring layer 15 in the horizontal direction and a second wiring layer 16 in the vertical direction, with these wiring layers 15 and 16 being electrically connected by a connection pattern 17. These are wiring patterns for making electrical connections between points A and B, and C and D.

[0004]

[Problems Which the Present Invention Attempts to Solve]

With a conventional automatic layout method for semiconductor integrated circuits such as this, wiring is only implemented on either a horizontal-direction or vertical-direction lattice member 11 or 12, even when using three or more wiring layers. Therefore, even when the number of wiring layers is increased, all that happens is that wiring is made easier, and wiring

length is hardly shortened at all, which constitutes a problem.

[0005]

An object of the present invention is to provide an automatic layout method for semiconductor integrated circuits wherein wiring length is shortened and the problem noted above is resolved.

[0006]

[Means Used to Solve the Abovementioned Problems]

The automatic layout method for semiconductor integrated circuits of the present invention is configured so as to employ a wiring layer using wiring on at least one horizontal-direction lattice member, a wiring layer using wiring on at least one vertical-direction lattice member, and a wiring layer using wiring on at least one diagonal-direction lattice member.

[0007]

[Embodiments]

Fig. 1 is a diagram of a wiring lattice used in a first embodiment of the present invention. In Fig. 1, in addition to horizontal-direction lattice members 1 and vertical-direction lattice members 2, diagonal-direction lattice members 3 that rise to the right and diagonal-direction lattice members 4 that decline to the right are established, and first, second, third, and fourth wiring layers are allocated as wiring layers used primarily in wiring on lattice members 1, 2, 3, and 4, respectively.

[0008]

Fig. 2 is a pattern diagram wherein a wiring pattern has been made using the lattice diagram of Fig. 1.

[0009]

In Fig. 2, there are a first wiring layer 7, a second wiring layer 8, a third wiring layer 5, and a fourth wiring layer 6, with an inter-wiring-layer connection pattern 9 provided at the connection points, etc.

[0010]

Fig. 2 shows an example of a wiring between point A and point B, and point C and point D. The wiring length is shorten by a factor of 0.7 to 0.8, compared to that of the conventional [wiring] shown in Fig. 4.

[0011]

[Benefits of the Invention]

The present invention, as described in the foregoing, by using wiring layers used in wiring on diagonal-direction lattice members in addition to wiring layers used in wiring on the usual horizontal- and vertical-direction lattice members, can shorten wiring lengths by a maximum factor of 0.7, providing the benefits of reduced wiring resistance and wiring capacitance, and faster operating speeds.

[Brief Description of the Drawings]

Fig. 1 is a diagram of a wiring lattice used with the automatic layout method for semiconductor integrated circuits in one embodiment of the present invention;

Fig. 2 is a diagram of a wiring pattern produced in conformity with the lattice diagrammed in Fig. 1;

Fig. 3 is a diagram of a wiring lattice used in a conventional automatic layout method; and

Fig. 4 is a diagram of a wiring pattern produced in conformity with the lattice diagrammed in Fig. 3.

[Explanation of Symbols]

1, 11 Horizontal-direction lattice members

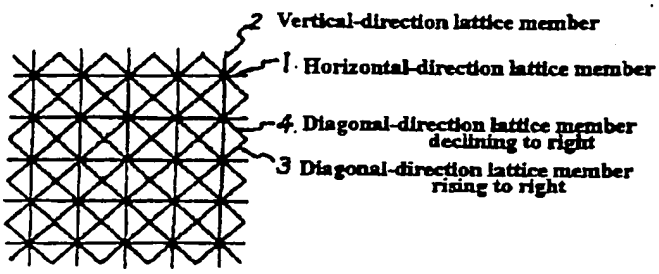
2, 22 Vertical-direction lattice members

3 Diagonal-direction lattice member rising to right

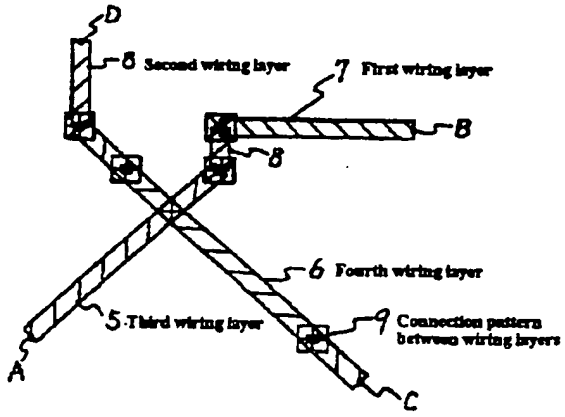
4 Diagonal-direction lattice member declining to right

5, 6, 15, 16 Wiring patterns between two points

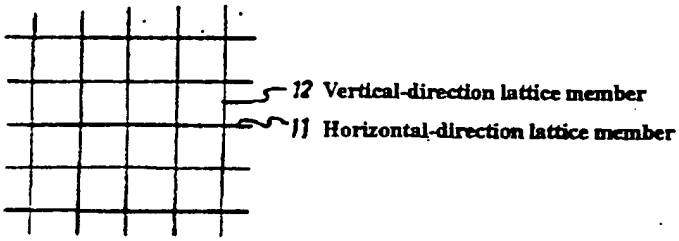
[Figure 1]



[Figure 2]



[Figure 3]



[Figure 4]